WHAT IS CLAIMED IS:

1. An integrated circuit comprising a memory array having at least one plane of memory cells, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, said NAND strings including a series select device at each end thereof.

2. The integrated circuit of claim 1 wherein the integrated circuit includes at least two memory planes formed above a substrate.

3. The integrated circuit of claim 1 wherein said switch devices include a charge storage dielectric.

4. The integrated circuit of claim 3 wherein said charge storage dielectric comprises an oxide-nitride-oxide dielectric stack.

5. The integrated circuit of claim 1 wherein said switch devices include a floating gate electrode.

6. The integrated circuit of claim 1 wherein adjacent NAND strings are respectively coupled to a respective global bit line by way of a respective zia structure having a pitch matching that of the adjacent NAND strings.

7. The integrated circuit of claim 1 further comprising a group of more than four adjacent NAND strings within the same memory block each associated with a respective global bit line not shared by the other NAND string of the group.

8. The integrated circuit of claim 1 further comprising NAND strings having an identical pitch as respective global bit lines associated therewith.

9. The integrated circuit of claim 1 wherein the memory cell devices and series selection devices forming each NAND string are structurally substantially identical.

10. The integrated circuit of claim 2 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

11. The integrated circuit of claim 2 wherein the substrate comprises a polycrystalline substrate.

12. The integrated circuit of claim 2 wherein the substrate comprises an insulating substrate.

13. The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

14. The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

15. The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

16. The integrated circuit of claim 1 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

17. The integrated circuit of claim 1 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.

18. An integrated circuit comprising a memory array having at least one plane of memory cells, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, having a group of more than four adjacent NAND strings within the same memory block each associated with a respective global bit line not shared by the other NAND string of the group.

19. The integrated circuit of claim 18 wherein the integrated circuit includes at least two memory planes formed above a substrate.

20. The integrated circuit of claim 18 wherein said switch devices include a charge storage dielectric.

21. The integrated circuit of claim 20 wherein said charge storage dielectric comprises an oxide-nitride-oxide dielectric stack.

22. The integrated circuit of claim 18 wherein said switch devices include a floating gate electrode.

23. The integrated circuit of claim 18 wherein adjacent NAND strings are respectively coupled to a respective global bit line by way of a respective zia structure having a pitch matching that of the adjacent NAND strings.

24. The integrated circuit of claim 18 further comprising NAND strings including a series select device at each end thereof.

25. The integrated circuit of claim 18 further comprising NAND strings having an identical pitch as respective global bit lines associated therewith.

26. The integrated circuit of claim 19 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

27. The integrated circuit of claim 19 wherein the substrate comprises a polycrystalline substrate.

28. The integrated circuit of claim 19 wherein the substrate comprises an insulating substrate.

29. The integrated circuit of claim 18 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

30. The integrated circuit of claim 18 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

31. The integrated circuit of claim 18 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

32. The integrated circuit of claim 18 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

33. The integrated circuit of claim 18 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.

34. An integrated circuit comprising a memory array having at least one plane of memory cells, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, having NAND strings on identical pitch as their respective global bit lines.

35. The integrated circuit of claim 34 wherein the integrated circuit includes at least two memory planes formed above a substrate.

36. The integrated circuit of claim 34 wherein said switch devices include a charge storage dielectric.

37. The integrated circuit of claim 36 wherein said charge storage dielectric comprises an oxide-nitride-oxide dielectric stack.

38. The integrated circuit of claim 34 wherein said switch devices include a floating gate electrode.

39. The integrated circuit of claim 34 wherein adjacent NAND strings are respectively coupled to a respective global bit line by way of a respective zia structure having a pitch matching that of the adjacent NAND strings.

40. The integrated circuit of claim 34 further comprising NAND strings including a series select device at each end thereof.

41. The integrated circuit of claim 34 further comprising a group of more than four adjacent NAND strings within the same memory block each associated with a respective global bit line not shared by the other NAND string of the group.

42. The integrated circuit of claim 35 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

43. The integrated circuit of claim 35 wherein the substrate comprises a polycrystalline substrate.

44. The integrated circuit of claim 35 wherein the substrate comprises an insulating substrate.

45. The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

46. The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

47. The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

48. The integrated circuit of claim 34 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

49. The integrated circuit of claim 34 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.